REPLY

To: Examiner of the Patent Office

1. Identification of the International Application
PCT/JP2004/004072

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5. Subject Matter of Reply:

This is a reply to the first Written Opinion mailed May 25, 2004.

The applicant has amended claim 1 with the Amendment separately filed.

D1 (JP2001-217442A) discloses a solar cell having an n-type polycrystalline silicon layer on a SUS substrate. However, the feature of the present invention resides in that a solar cell comprises a non-doped layer stacked on a silicon substrate, the layer having an amorphous silicon phase and a microcrystalline silicon phase mixed together, and the silicon substrate is formed by stacking a high-purity polycrystalline silicon layer on a base composed of a

polycrystalline metal-grade silicon solidified in one direction. Accordingly, the solar cell of the present invention comprising the non-doped layer formed on the substrate is neither disclosed nor suggested by the solar cell of D1 comprising n-type layer, i.e., the doped layer formed on the substrate.

D2 (JP3-228324A) discloses that a first insulating layer, a first polycrystalline layer and a second insulating layer are formed in the mentioned order on a metallurgical silicon substrate by CVD, and then the first polycrystalline layer is crystallized by thermal energy and then the second insulating layer is removed. D2 discloses that a second polycrystalline layer is grown in liquid phase on the formed first polycrystalline layer (see Fig. 2). Accordingly, the solar cell of the present invention comprising a non-doped layer having an amorphous silicon phase and a microcrystalline silicon phase mixed together as a layer formed on the substrate is neither disclosed nor suggested by the solar cell of D2 comprising the first insulating layer, the first polycrystalline layer and the second semiconductor layer, which do not an amorphous silicon phase and a microcrystalline silicon phase mixed together, as a layer formed on the substrate.

D3 (JP2001-332494A) discloses a process for fabricating a semiconductor device comprising a step of forming a crystalline silicon layer composed of polycrystalline silicon or microcrystalline silicon on a substrate, a step of forming an amorphous silicon layer on the crystalline layer, and a step of crystallizing the

amorphous silicon layer by irradiating the the surface of the amorphous silicon layer with a laser beam. Accordingly, the solar cell of the present invention comprising the non-doped layer, formed on the substrate, having an amorphous silicon phase and a microcrystalline silicon phase mixed together is neither disclosed nor suggested by the semiconductor of D3 having no amorphous silicon layer as a final product.

D4 (JP9-312258A) discloses that a thin layer of amorphous or microcrystalline silicon is formed on a substrate in an intermediate step. However, the semiconductor device of D4 as the final product does not contain an amorphous or microcrystalline silicon layer and the substrate of D4 is not metal-grade silicon. From these differences, the present invention is neither disclosed nor suggested by D4.

As described above, the present invention of amended claim 1 is nether disclosed nor suggested by D1 to D5, alone or in combination, and therefore amended claim 1 possesses novelty and inventive step.